DIGITAL CONTROL OF DUAL-LOAD LCLC RESONANT CONVERTERS

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Abstract

The paper proposes the analysis, design and realisation of dual-output resonant LCLC converters with independent output regulation, employing a single power stage and combined PWM and frequency control. Asymmetric switching of the power devices is used to facilitate independent control of the outputs to provide +5V and +3.3V from a 15V-20V input supply over a range of load conditions.

Introduction

There is increasing interest in the provision of power supply technologies that provide multiple outputs—typical growth areas being the telecommunications, computer and microprocessor industries where mobile phones, PDAs and handheld products typically require 3.3V, 5V, 12V and 15V supplies for various interfaces. Enabling technologies such as high frequency, high power switching devices and low cost digital control system has spawned significant interest on resonant converters as possible candidates for such DC-DC converters, delivering independently stabilized outputs. Analytical work on the behaviour of multi-output series resonant converters (SRC), has been presented in [1, 2]. However, only one of these outputs is normally regulated through feedback control, with the remainder being either unregulated or secondary-side post regulated. A key drawback of such strategies, however, is the cross regulation error on the unregulated output that is subjected to frequency regulation. The treatment in [3] suggests the implementation of a PWM control technique to minimise poor cross regulation problems, whilst [4, 5] propose that use of a centre-tapped transformer that is terminated through two output windings, and full wave rectification. A major disadvantage of the suggested configuration, however, is the high rectifier diode count that accompanies the full bridge rectification, and, once again, recourse to a single closed-loop to regulate one output, is made.

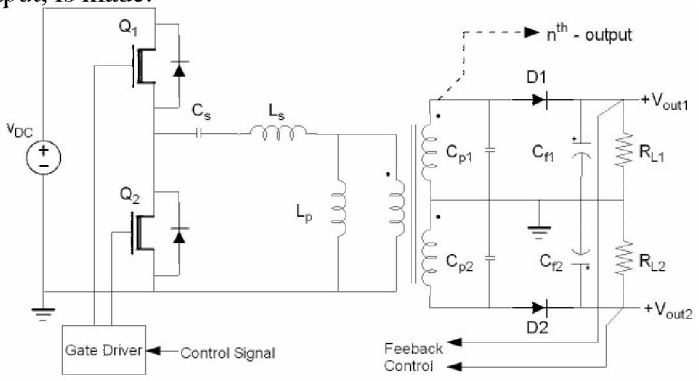

Fig. 1: Dual-load LCLC resonant converter with feedback control

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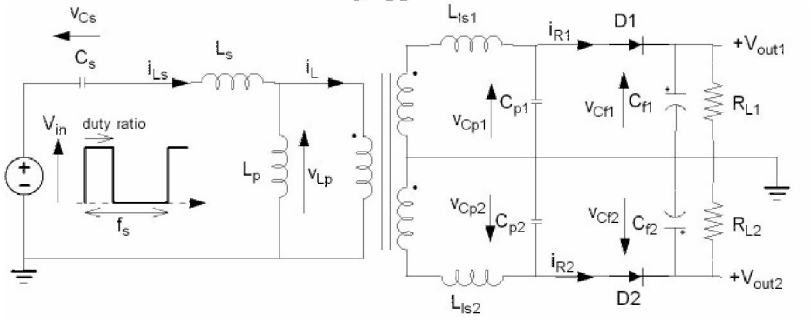
Here, the use of dual-output resonant LCLC converters, Fig. 1, that are excited asymmetrically through both duty-cycle and frequency control, to maintain a desired output voltage distribution, is proposed. A state variable model of the proposed converter is developed to aid in the design and analysis. Solutions generated from the state space model, are discussed, and compared with measurements from an experimental converter. The feasibility of the proposed converter is further underpinned by the development of a basic control scheme that yields stable system responses and excellent regulation behaviour on both outputs.

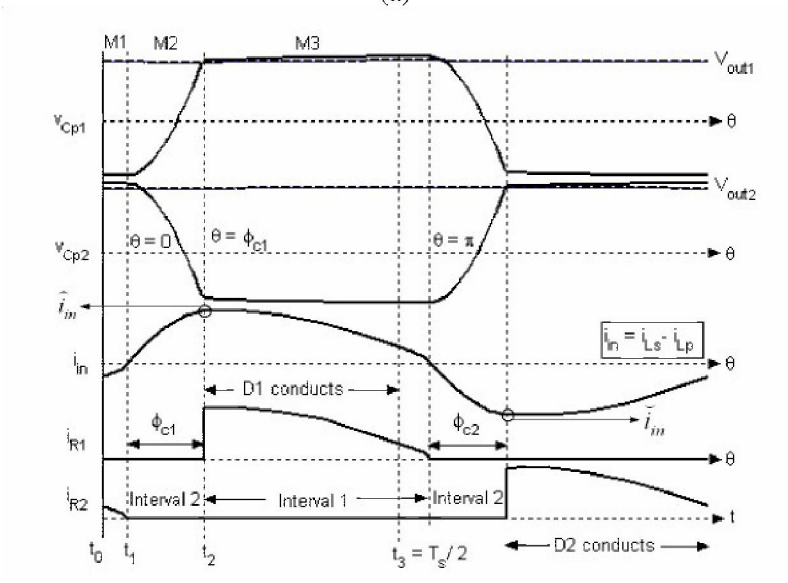
Circuit model of the dual-loads LCLC-SPRC

Design and analysis of fourth-order resonant converters with capacitive output filters, have been previously considered in [6]. From the results therein, it was shown that all variants provided beneficial attributes compared to 2nd-order SRC and PRC counterparts, by combining their best features, i.e. they can be regulated over a wide load range with reduced circulating power. Moreover, parasitic elements that are normally problematic for other converter designs can be readily absorbed into the resonant network to enhance performance and reduce mass and volume.

A schematic of a half-bridge LCLC-SPRC with two outputs is shown in Fig. 2(a). By changing the full bridge rectifier to a dual-complementary rectifier, the resulting dual-load converter combines the benefits of requiring a minimum number of rectifier diodes and the ability for multi-output regulation. The rectifier is most efficient under balanced high- and low-side output loading, and, is typically used together with capacitor-type output filters for low current rating applications.



(a)



(b)

Fig. 2: Dual-load 4th-order resonant converter (a) schematic (b) typical operating waveforms

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The transformer in Fig. 2(a) can be modelled as an ideal voltage conversion component with a magnetising inductance, L_m, series primary leakage inductance, L_{lp} and secondary series leakage inductances, L_{ls1} and L_{ls2}. Since the primary leakage inductance of a well-designed ferrite transformer is much smaller than the magnetising inductances, L_m, it can be absorbed into the resonant tank series inductor, L_s. The value of the series resonant inductance can be increased by adding discrete components, if required, to satisfy pre-determined design constraints.

To demonstrate the ability of the converter to deliver unsymmetrical output voltages, under balanced load conditions, the transformer is constrained to have unity turns-ratios on both output windings, and the high- and low-side parallel resonant capacitors, C_{p1} and C_{p2}, are selected to have identical values. The output filter capacitors, C_{f1} and C_{f2}, are assumed to be large enough so the voltages they are subjected to can be considered constant over a switching period.

Since current flows through the primary side of the transformer to the top- and bottom-sides of the rectifier, during different half-cycles of tank excitation, see Fig. 2(b), each output is replenished with energy alternately. During the positive half-cycle of the parallel resonant capacitor voltage waveform, v_{Cp}, the resonant current flows toward the top-side rectifier through to output, R_{L1}, resulting in the voltage V_{out1}; whilst the resonant current then supplies power to V_{out2} when the polarity of the resonant capacitor voltage changes polarity. Diodes D1 and D2 clip the parallel capacitor voltage to $+V_{out1}$ or $-V_{out2}$.

Classically, either the high-side or low-side output will be closed-loop regulated through frequency modulation. However, variations in line voltage or load resistance then yield cross regulation errors [1, 2] on the unregulated output. Moreover, an asymmetric output voltage distribution cannot be achieved, in general, under balanced output load conditions, regardless of switching frequency. It is therefore proposed that the converter is operated asymmetrically through variation of input voltage duty cycle, and frequency, to facilitate regulation of both output voltages.

State-variable analysis of dual-load resonant converter

A state-variable model describing the behaviour of the dual-load converter can be obtained by considering the electrical network in Fig. 2. The model is derived by separating the converter dynamics into 'fast' and 'slow' sub-systems, with their interaction related by a set of coupling equations. The leakage inductance of a well-designed ferrite transformer is normally small compared to its magnetising inductance. For this reason, its effect are neglected, for brevity. State variables are selected based on voltages and currents that govern the operation of the resonant tank. The fast sub-system is therefore considered to describe the dynamics of the resonant tank and power switches (1)—the underlying equations exclude the effects of parasitics.

$$\frac{di_{Ls}}{dt}=\frac{V_{in}-v_{Cs}-v_{Lp}}{L_s} \qquad \frac{di_{Lp}}{dt}=\frac{v_{Lp}}{L_p}$$

$$\frac{dv_{Cs}}{dt}=\frac{i_{Ls}}{C_s} \qquad \frac{dv_{Cp1}}{dt}=\frac{i_{Ls}-i_{Lp}-i_{R1}-i_{Cp2}-i_{R2}}{C_{p1}} \qquad \frac{dv_{Cp2}}{dt}=\frac{i_{Ls}-i_{Lp}-i_{R1}-i_{Cp1}-i_{R2}}{C_{p2}} \qquad (1)$$

As discussed previously, the path of the current leaving the transformer secondary windings changes during the positive and negative half-cycles of the parallel capacitor voltage, due to the effect of the rectifiers allowing current to conduct only in single direction. During the positive half-cycle interval, D_1 is forward biased and permits the rectifier current i_R to supply the load R_{L1}. During the negative half-cycle the top rectifier is reverse-biased and D_2 supports power transfer to load R_{L2}.

If the output filter capacitors are assumed to be sufficiently large so as to maintain a constant voltage on both outputs over a switching period, their contribution to the dynamics is given by:

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$$\frac{dv_{cf1}}{dt}=\frac{i_{R1}}{C_{f1}}-\frac{v_{cf1}}{C_{f1}R_{L1}} \qquad \frac{dv_{cf2}}{dt}=\frac{i_{R2}}{C_{f2}}-\frac{v_{cf2}}{C_{f2}R_{L2}} \tag{2}$$

As discussed, during interval $t_1 \rightarrow t_2$ (see Fig. 2(b)) the parallel resonant capacitor voltage is clamped to output voltage, v_{cf1} during the positive half-cycle, and conversely, to $-v_{cf2}$ during the negative half-cycle, due to the action of the rectifiers. By noting that there will be negligible current flowing through C_p during these periods, the rectifier input voltage is dependent on the direction of the current leaving the resonant tank inductances, i.e. $i_L = i_{Ls} - i_{Lp}$. The relevant coupling terms are therefore obtained by equating voltages at either side of the rectifier, for each respective half-cycle, as follows:

$$\begin{aligned} v_{Cp1} &= \mathrm{sgn}(i_L)(V_{out1}+v_{diode}) = \mathrm{sgn}(i_L)(v_{cf1}+v_{diode}) \\ v_{Cp2} &= \mathrm{sgn}(i_L)(V_{out2}+v_{diode}) = \mathrm{sgn}(i_L)(v_{cf2}+v_{diode}) \end{aligned} \tag{3}$$

Assuming a constant rectifier on-state voltage, differentiating (3) gives:

$$\frac{dv_{Cp1}}{dt}=\mathrm{sgn}(i_L)\frac{dv_{cf1}}{dt} \qquad \frac{dv_{Cp2}}{dt}=\mathrm{sgn}(i_L)\frac{dv_{cf2}}{dt} \tag{4}$$

Consider the rectifier current, i_{R2}, is zero during the positive half-cycle of the parallel capacitor voltage. Equations (1) and (2) can be substituted into (4) and solved for the rectifier current i_{R1},

$$i_{R1}=\frac{C_{p1}C_{f1}}{\mathrm{sgn}(i_L)C_{p1}+C_{f1}}\left(\frac{i_L-i_{Cp2}-i_{R2}}{C_{p1}}+\frac{\mathrm{sgn}(i_L)v_{cf1}}{C_{f1}R_{L1}}\right) \tag{5}$$

This leads to the following coupling equations describing the rectifier currents within each half of a switching cycle:

$$i_{R1}=\begin{cases}\dfrac{C_{p1}C_{f1}}{\mathrm{sgn}(i_L)C_{p1}+C_{f1}}\left(\dfrac{i_L-i_{Cp2}-i_{R2}}{C_{p1}}+\dfrac{\mathrm{sgn}(i_L)v_{cf1}}{C_{f1}R_{L1}}\right) & \text{for } v_{Cp1}=V_{out1}+v_{diode} \\ 0 & \text{for } v_{Cp1}<V_{out1}+v_{diode}\end{cases}$$

$$i_{R2}=\begin{cases}\dfrac{C_{p2}C_{f2}}{\mathrm{sgn}(i_L)C_{p2}+C_{f2}}\left(\dfrac{i_L-i_{Cp1}-i_{R1}}{C_{p2}}+\dfrac{\mathrm{sgn}(i_L)v_{cf2}}{C_{f2}R_{L2}}\right) & \text{for } v_{Cp2}=V_{out2}+v_{diode} \\ 0 & \text{for } v_{Cp2}<V_{out2}+v_{diode}\end{cases} \tag{6}$$

Assuming the effect of transformer output leakage inductances are negligibly small i.e. L_s, C_s, L_p and C_p dominate behaviour, the voltage across L_p is assumed to be a reflection of the voltages across C_{p1} and C_{p2}, and the state vector for the parallel inductor current in the fast sub-system (see Equation (1)) simplifies to $v_{Lp} = v_{Cp}$. It is noted that C_{p1} and C_{p2} charging/discharging currents are similar, implying that current flowing from the primary side of the transformer is equally shared between them. In this case, the shunt connection of the parallel resonant capacitors can also be used to conveniently include the effects of the transformer output stray capacitances or output rectifier diode junction capacitances. The state variable equations for the parallel resonant capacitor voltage (1) can be simplified to:

$$\frac{dv_{Cp1}}{dt}=\frac{i_{Ls}-i_{Lp}-i_R}{2C_{p1}} \qquad \frac{dv_{Cp2}}{dt}=\frac{i_{Ls}-i_{Lp}-i_R}{2C_{p2}} \tag{7}$$

The state-variable equations are readily employed in MATLAB/SIMULINK to investigate the behaviour of an example dual-loads converter when subject to asymmetrical input excitation, with balanced output loads. The converter is powered from 30V DC-link. Model parameters for the simulations are given in Table I. A resulting plot of the steady-state output voltage characteristics, V_{out1} and V_{out2}, as a function of switching frequency and duty-cycle ratio, is given in Fig. 3 (the secondaries of the transformer have

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identical turns ratios, and the parallel resonant capacitances are the same). From Fig. 3, it is evident that for operation above resonance, the sum of the output voltages applied to the loads increases as the operating frequency tends to the effective resonant frequency, for fixed values of duty ratio. Furthermore, for 50% duty ratio, giving symmetric square-wave excitation of the tank, the converter delivers identical voltages to both high- and low-side outputs, for fixed operating frequencies, as expected.

For a given a particular operating frequency, a decrease in the duty ratio, from 50%, is seen to deliver more energy from the resonant tank to energize output V_{out1}, thereby yielding a correspondingly higher output voltage, and power. Conversely, increasing the duty ratio beyond 50% is seen to deliver more power to the secondary winding to support a higher V_{out2}. From this characteristic, it is clear that, for balanced loads, the voltage and power distribution to each output can be independently influenced by suitable choice of duty ratio and switching frequency. Furthermore, it can be seen that the slope of the curves, Figs. 4(a) and (b), are greater for lower values of switching frequency. This implies that when a large difference between the output voltages is required, the converter should be operated close to resonance, leading to high efficiency operation, and zero voltage switching. However, this also means that the tank components are subjected to higher electrical stresses.

Table I Converter model parameters

Parameters	Values
Resonant frequency, f_o (kHz)	130
Resonant capacitance ratio, C_n	0.03
Resonant inductance ratio, L_n	0.01
Series load quality factor, Q_{op1}	6

Figure 5(a) shows the relative voltage distributions as a function of the ratio of the input voltage duty, and load quality factor, Q_{op1}. It can be seen that the slope of the characteristic is relatively independent of the quality factor, for high Q_{op1}, although the attainable difference between the output voltages is seen to be greater for low values of load quality factor. Hence, operation with low Q_{op1} should be chosen to facilitate large voltage differences, as opposed to use of high Q_{op1} to facilitate sinusoidal tank currents and voltages. Moreover, low Q_{op1} conditions implies that the output voltage vs. frequency behaviour of the converter has a 'flatter' characteristic, and a greater range of switching frequencies are required to regulate the output voltage when the converter is subjected to variations in DC-link voltage or load, thereby requiring greater controller effort and bandwidth for tracking control [6]. A trade off is therefore required in the selection of the key converter parameters.

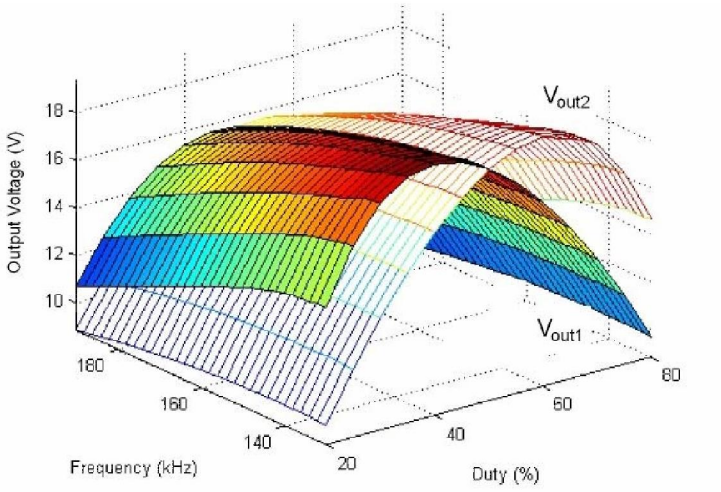

Fig. 3 Output voltages distribution vs. switching frequency and duty ratio

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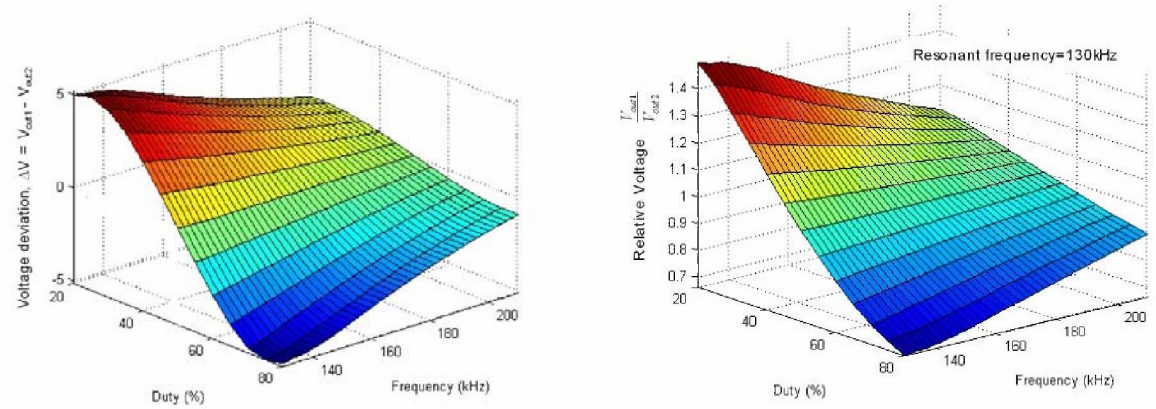
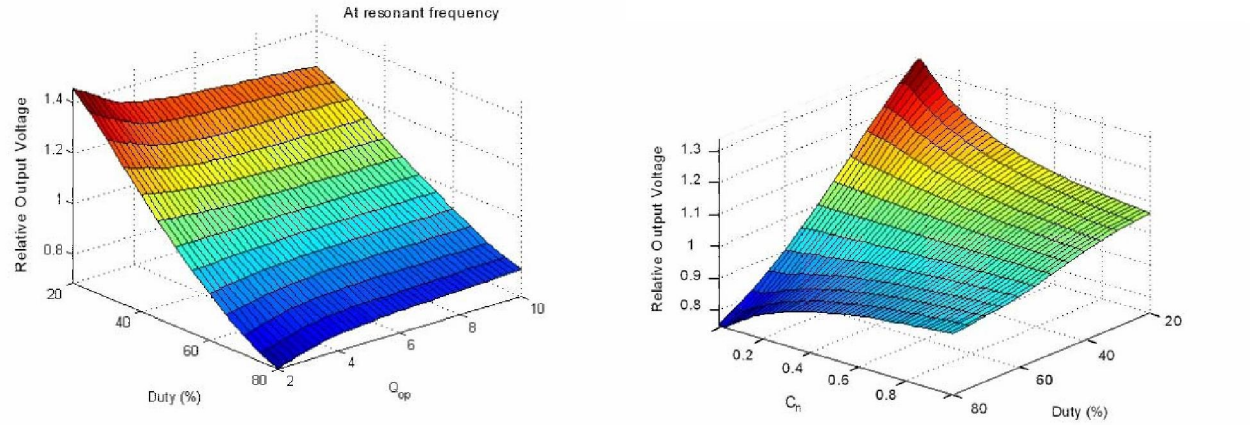
It is instructive to show the impact of converter parameters on the attainable voltage distributions. Fig. 5(b) therefore shows an example of the resulting voltage distribution, as a function of duty ratio, as resonant capacitance ratio C_n is varied. It can be seen, in particular, that the slope of the characteristic is greater for low ratios of resonant capacitance. Hence, it is instructive to choose a low value for C_n ratio during the design phase. However, a choice of low parallel capacitance means the input-output voltage characteristic exhibits a reduced resonant peak, and consequently, the voltage boosting capability of the converter is limited. Furthermore, the input-output voltage conversion ratio, at the effective resonant frequency of the tank, is consequently lower, and the resulting converter therefore appears more suitable for step-down DC-DC applications.



(a) (b)

Fig. 4 Asymmetrical voltage distribution: a) Output voltages deviation, b) relative voltage distribution



(a) (b)

Fig. 5 Converter characteristics as a function of a) duty ratio and Q_{op1} and, b) duty ratio and C_n

Figures 3 to 5 have established that a chosen distribution of output voltages (with balanced loads) can be maintained using a combination of switching frequency and duty ratio control, so long as the maximum deliverable voltage, and input voltage vs. input current phase angle, are not exceeded. For the particular converter example considered, Table II lists example operating conditions for providing various output voltage distributions, with the DC-link fixed at v_{DC}=30V.

Theoretically, a controlled variation in the output voltages, as shown in Fig. 3, can be obtained by operating the converter around a designated point in the region of high gradient on the frequency characteristic. However, high efficiency soft-switching operation cannot be sustained if the converter is

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operated at resonance, to obtain the maximum output voltage difference. As a result, the switching frequency must be constrained to preserve Zero Voltage Switching (ZVS).

Table II Example output voltage distributions

f_s (kHz)	*Duty* (%)	V_{out1} (V)	V_{out2} (V)	i_{Ls} (A)	v_{Cs} (V)	$\Delta\beta_{in}$ (°)	ϕ_{c1} (°)	ϕ_{c2} (°)
145	20	15V@20W	10V@10W	7.15	8	0	53.8	51.3
145	80	10V@10W	15V@20W	4.84	25.6	64.5	51.4	53.9
205	50	15V@25W	15V@25W	5.69	16.99	47	59	59

Fig. 6 shows an example input voltage vs. input current, phase difference, $\Delta\beta_{in}$, for the example converter, plotted against the normalised switching frequency $\omega_n = \omega_s/\omega_o$ and input voltage duty-ratio. At frequencies less than the tank resonant frequency, the input impedance of the tank network Z_{in} is dominated by the tank capacitance. Hence, the input switch current fundamental component leads the input voltage and the resonant tank presents an effective capacitive load. This provides Zero Current Switching (ZCS) for $\Delta\beta_{in} < 0$. When the resonant converter is operated above resonance, Zero Voltage Switching (ZVS) occurs, and the resonant tank presents an effective inductive load to the half-bridge switches, and the switch current lags the switch voltage.

At the effective resonant frequency, ω_o under asymmetric square-wave input voltage excitation, the input voltage lags the first harmonic of the input current, $\Delta\beta_{in} < 0$ when the duty cycle falls below 50%—see Fig. 7. The condition for inductive mode conduction of resonant converter, under asymmetric conditions, is therefore expressed as,

$$\Delta\beta_{in} = \beta_{in} - \phi_{vi(1)} \geq 0 \tag{8}$$

where $\Delta\beta_{in}$ is the phase angle between the actual square input voltage and fundamental of the input current; β_{in} is the phase lag between the first harmonic of the input voltage and current; and $\phi_{vi(1)}$ is phase of the fundamental frequency component of the input voltage, $v_{i(1)}$. (Noting that β_{in}=0 at resonance, and $\beta_{in} > 0$ above resonance, implies that the first harmonic of the input voltage leads the first harmonic of the current).

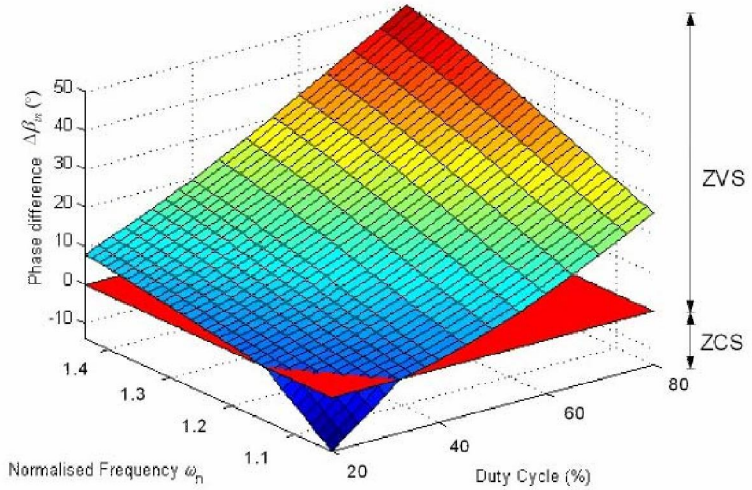

Fig. 6 Phase difference $\Delta\beta_{in}$ versus the normalised switching frequency and duty ratio

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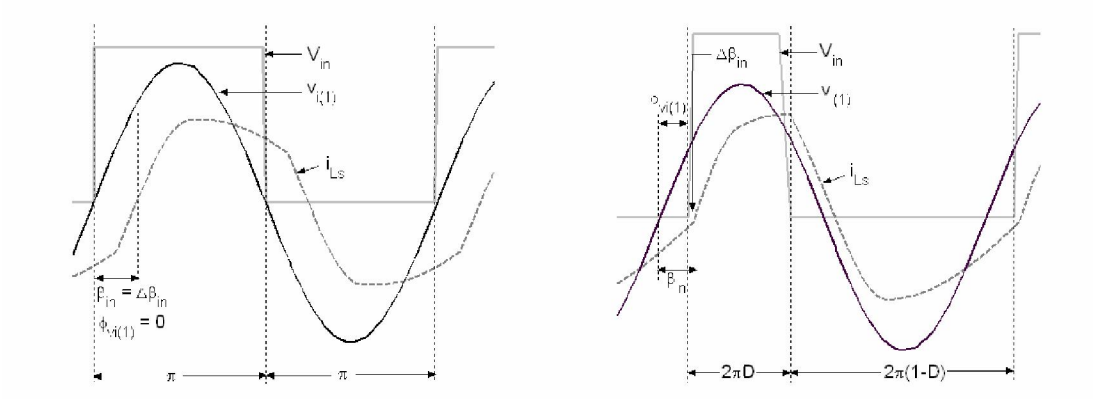
For asymmetrical operation of the converter, Fig. 7(b), the duty-cycles of Q_1 and Q_2 are denoted, respectively, D and 1-D, where D is the ratio of the turn-on period with respect to the switching period. Asymmetric switching therefore provides an asymmetrical voltage source V_{in} to excite the tank, of amplitude v_{DC}:

$$V_{in} = \begin{cases} v_{DC} & \theta = 0 \ldots 2\pi D \\ 0 & \theta = 2\pi D \ldots 2\pi \end{cases} \tag{9}$$

Assuming that only the fundamental component excites the resonant tank, the first harmonic of the resulting input voltage, $v_{i(1)}$, and its phase angle, $\phi_{vi(1)}$ are given by:

$$v_{i(1)} = \frac{2v_{DC}}{\pi}\sqrt{1-\cos(2\pi D)} \times \sin\left(\omega t + \phi_{vi(1)}\right) \qquad \phi_{vi(1)} = \frac{\pi}{2} - \pi D \tag{10}$$

The condition for inductive switching can now be re-written as $\beta_{in} \geq \pi(0.5-D)$, which is obtained by increasing the switching frequency to give an increase in $\Delta\beta_{in}$. However, this will induce higher circulating currents that increases conduction losses and contributes to thermal problems. Increasing the switching frequency also compromises the ability of the converter to deliver wide voltage differences between the high- and low-side outputs. The converter should therefore be ideally operated at the minimum switching frequency, above resonance, that can achieve ZVS.



(a) (b)

Fig. 7 Waveforms of V_{in}, $v_{i(1)}$ and i_{Ls} at (a) D=0.5 ($\Delta\beta_{in} = \beta_{in}$) and (b) D=0.3 ($\Delta\beta_{in} < \beta_{in}$)

Closed-loop Control and Experimental Realisation

Results of the possible output voltage distributions available from the dual-output converter, Table II, have demonstrated the dependence of the output voltages on both the duty-ratio and switching frequency. The objective, for control purposes, is to force the converter outputs to the set points in the presence of line voltage and load disturbances. Fig. 8(a) shows the structure for the proposed controller, employing two decoupled feedback loops for independent control of frequency and duty-ratio. Voltage feedback modulation is employed to avoid the need for relatively expensive current sensors, and the control structures are based on linear Proportional and Integral (PI) schemes, as a proof of principle. For design purposes, the output voltage vs. switching frequency and duty-ratio characteristics of the converter, are approximated to be linear over the frequency range of interest.

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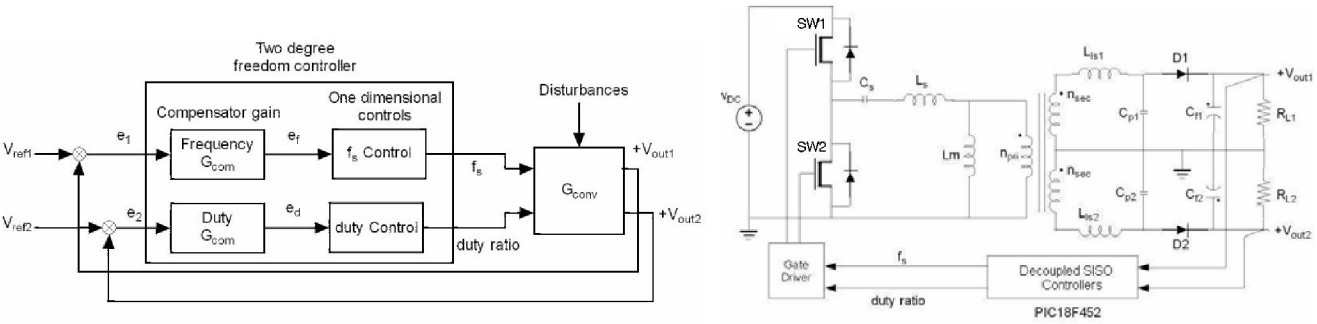

Fig. 8 Dual-load converter (a) Closed-loop controller structure (b) Schematic diagram of converter

Although various methodologies can be considered for the design of the PI gains, the controller parameters have been selected empirically for robust tracking of the reference. The digital compensator is tuned to respond quickly to variations of V_{out1}, whilst the controller reacting to variations of V_{out2}, acts relatively slowly—thereby effectively decoupling the interaction of the control loops. The switching frequency is restricted to values above the effective resonant frequency to maintain high efficiency operation. A block diagram of the digitally-controlled converter is shown in Fig. 8(b), and comprises of a PIC18F452-based interface—an 8-bit fixed-point microcontroller that is optimized for low-cost, and integrates 10-bit analogue-digital converters with high sampling rates. The control outputs from the PIC microcontroller are the effective turn-ON and turn-OFF times of the power switches, which are latched into registers on a SPARTAN-2 FPGA. The FPGA is used to derive signals for switching of the power devices.

Table III Prototype dual-loads converter specification and component values

Parameter	v_{DC} (V)	L_s (μH)	C_s (μF)	C_{p1} (μF)	C_{p2} (μF)	R_L (Ω)	L_m (μH)
Value	15	1.55	1.5	0.116	0.116	4	109

A prototype converter (see Table III for parameters) is designed using the procedure given in [6] to provide regulated +5V and +3.3V outputs from a DC-link input voltage in range 15V to 20V. The realisation of the converter along with control circuitry, is shown in Fig. 9(a). Investigations have been undertaken using an experimental setup that allows load changes within the range 3Ω to 6Ω, to be applied. Fig. 9(b) shows the resulting steady-state error between the reference voltages, V_{ref1} and V_{ref2} and the resulting measured output voltages of the converter, over the specified range of DC-link input voltages (15V to 20V) with a 5Ω load.

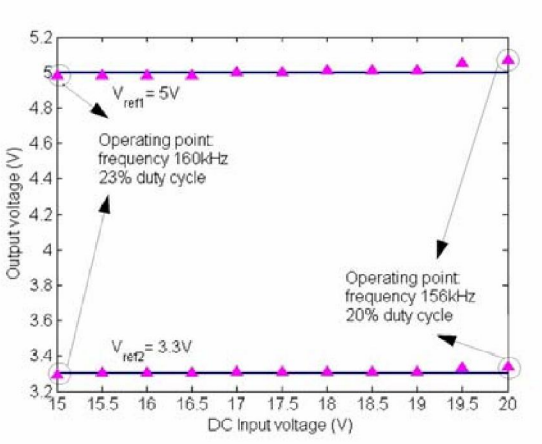

Fig. 9 Practical 4th-order dual-output resonant converter (a) photograph (b) Input voltage variation

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Figure 10 shows the response of the converter resulting from transient start-up conditions, for a range of applied input voltages and output voltage distributions. It can be seen that the converter voltages converge rapidly to the reference values, with an initial overshoot of ~10%. The overshoot is attributable to initial saturation of the integral action of the controller. Nevertheless, the response of the controller is deemed satisfactory in each case.

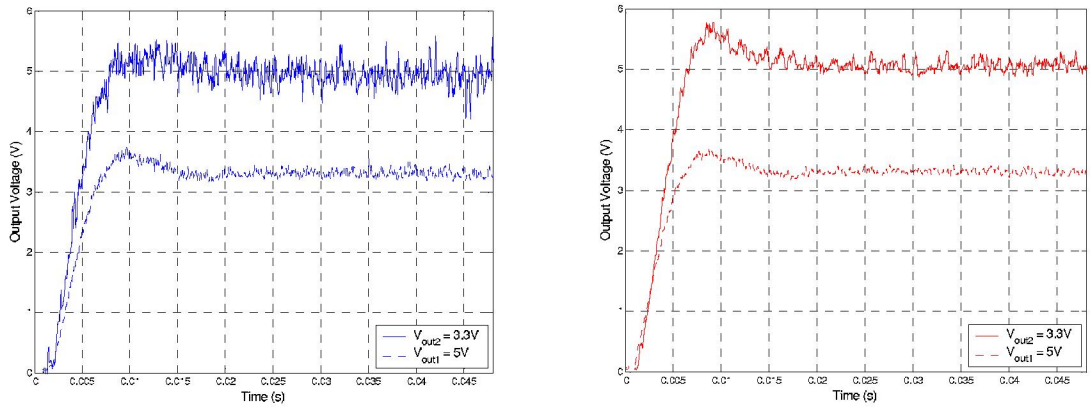

Fig. 10 Start-up transient response for various combinations of output voltage distributions and DC-link input voltages (a) v_{DC}=15V, V_{out1}=5V, V_{out2}=3.3V; (b) v_{DC}=20V, V_{out1}=5V, V_{out2}=3.3V

Conclusion

The characteristics of the dual-load, 4th-order LCLC voltage-output resonant converter, have been explored. It has been demonstrated that the two outputs of the converter can be independently regulated to provide asymmetrical output voltage distributions. A comparison of measurements from a prototype converter, capable of delivering 5V and 3.3V suitable for a standard electronic supply, with those from a derived state-variable model, and SPICE simulations, shows that the model provides accurate predictions of output voltage under steady state conditions. Moreover, a basic control scheme is shown to allow reliable regulation of both outputs under transient start-up conditions.

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